

FIG. 1A

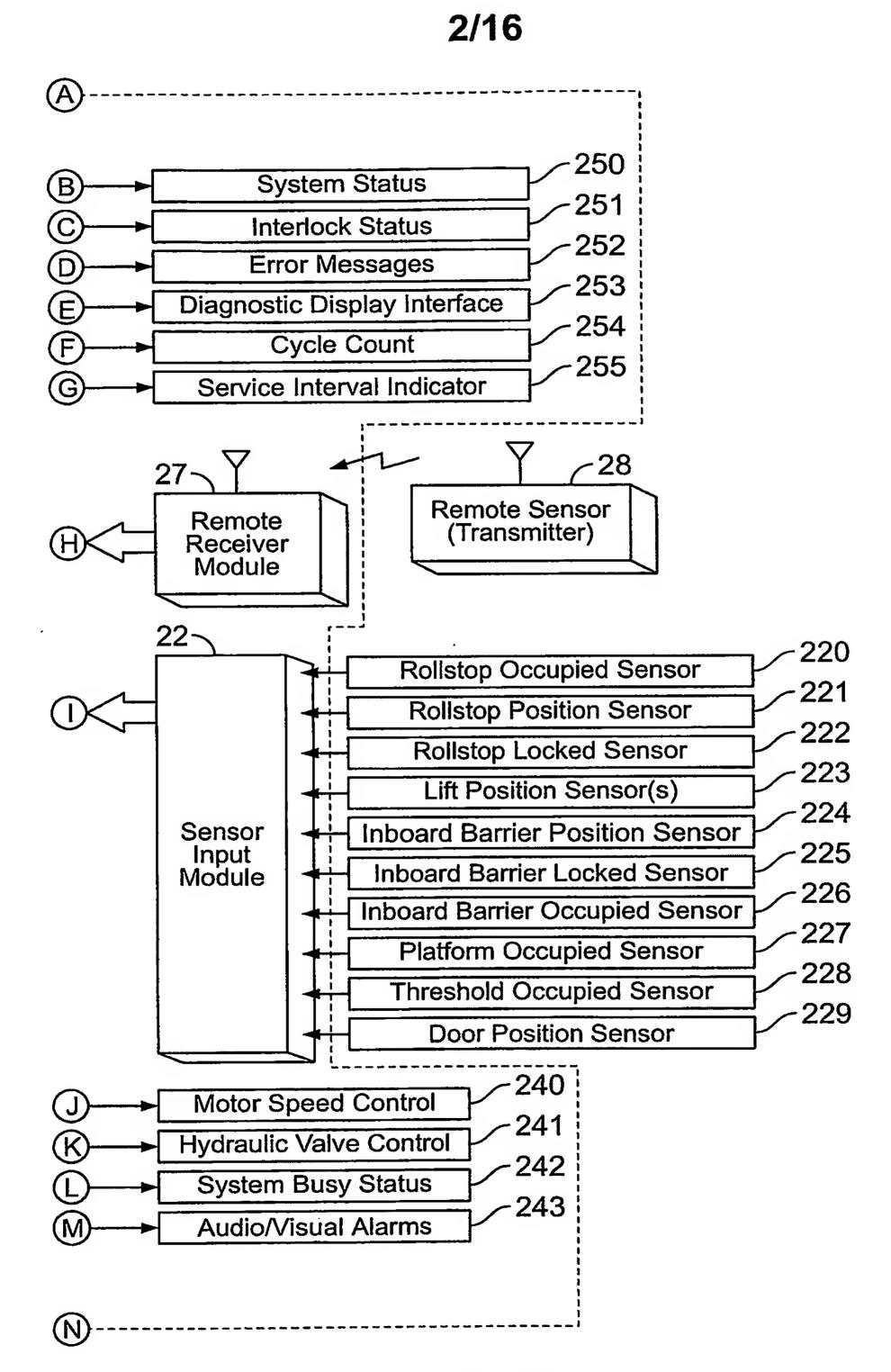
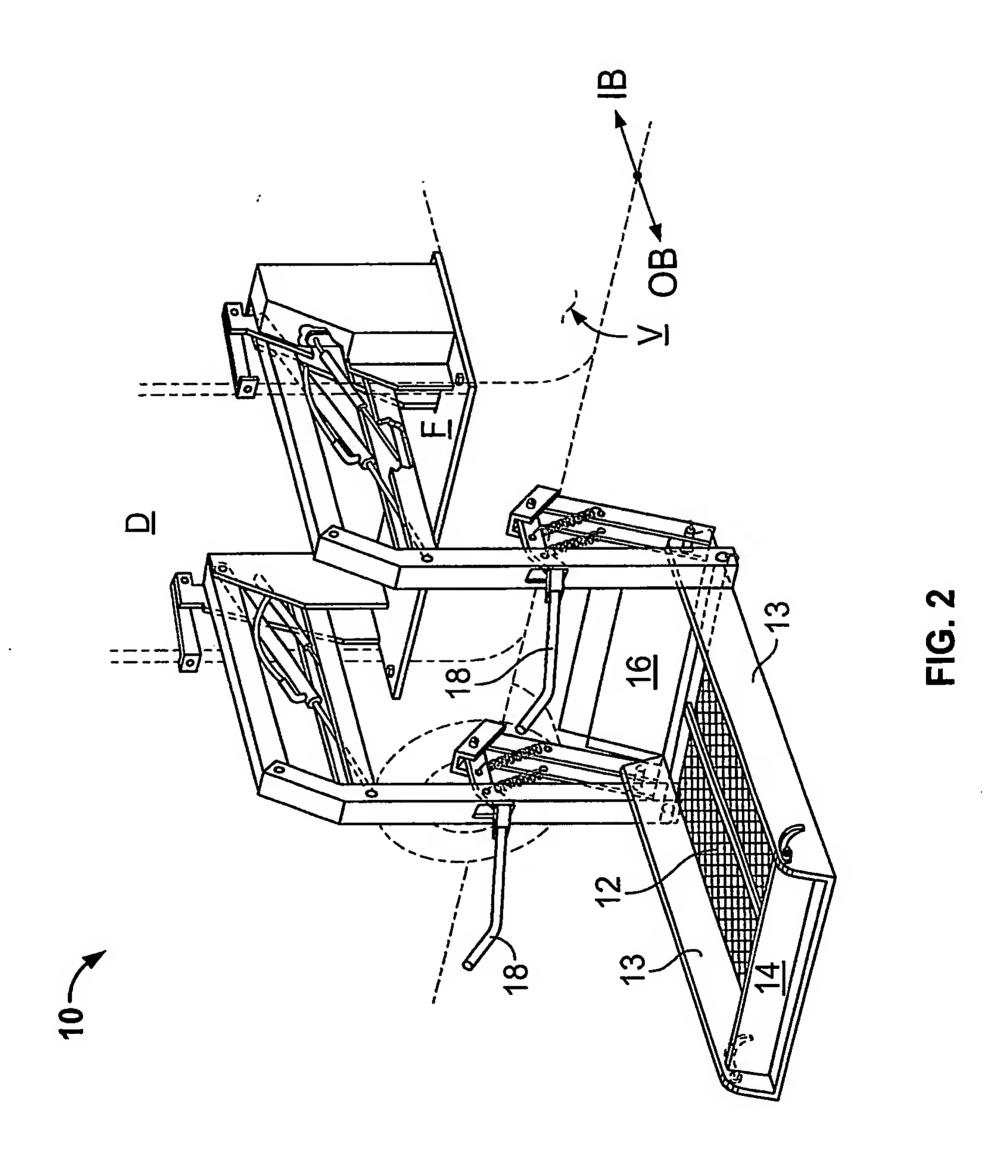
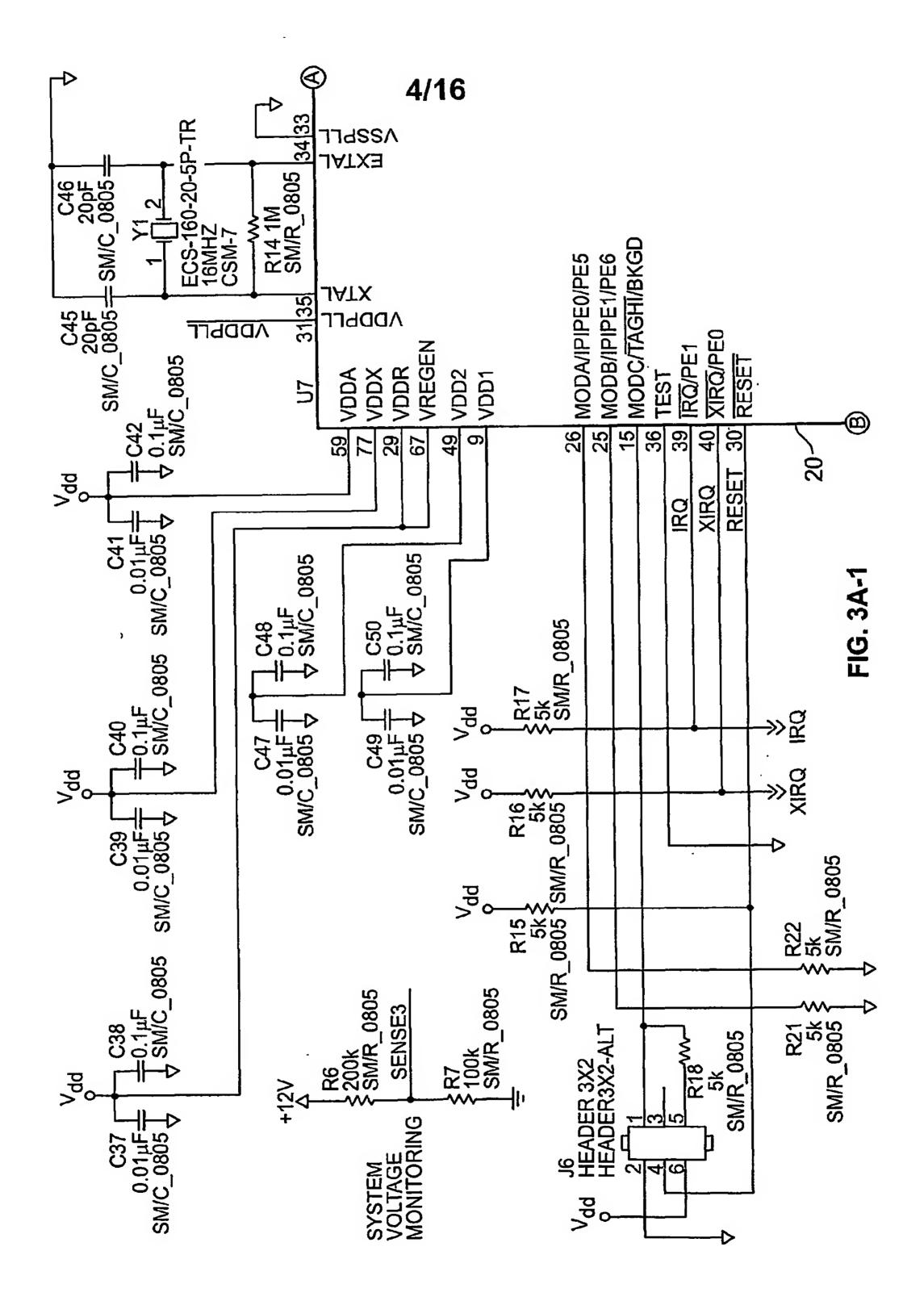


FIG. 1B

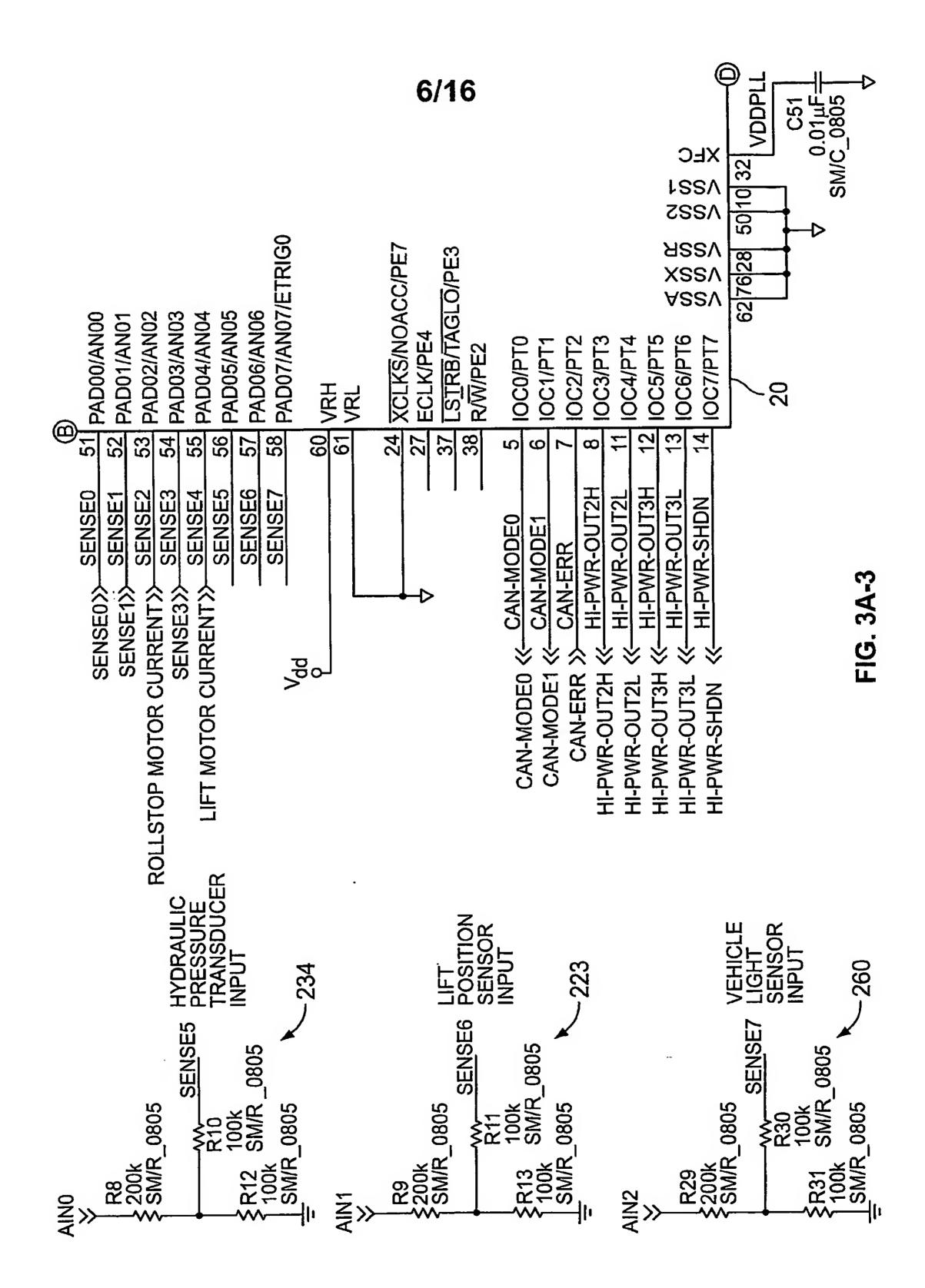
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		H.
		Vdd R20 \$ 5k \$ SM/R_0805 << IIC-DATA << IIC-CLOCK
ADDR0/DATA0/PB0 ADDR1/DATA1/PB1 ADDR2/DATA2/PB2 ADDR3/DATA3/PB3 ADDR3/DATA3/PB3 ADDR5/DATA5/PB5 ADDR5/DATA5/PB5 ADDR5/DATA5/PB5 ADDR5/DATA5/PB5 ADDR5/DATA5/PB5 ADDR5/DATA5/PB5	<u> </u>	ADDR12/DATA12/PA4 ADDR13/DATA13/PA6 ADDR14/DATA14/PA6 ADDR15/DATA15/PA7 ADDR15/DATA15/PA7 TXCAN4/SDA/KWJ6/PJ6 TXCAN4/SCL/KWJ7/PJ7

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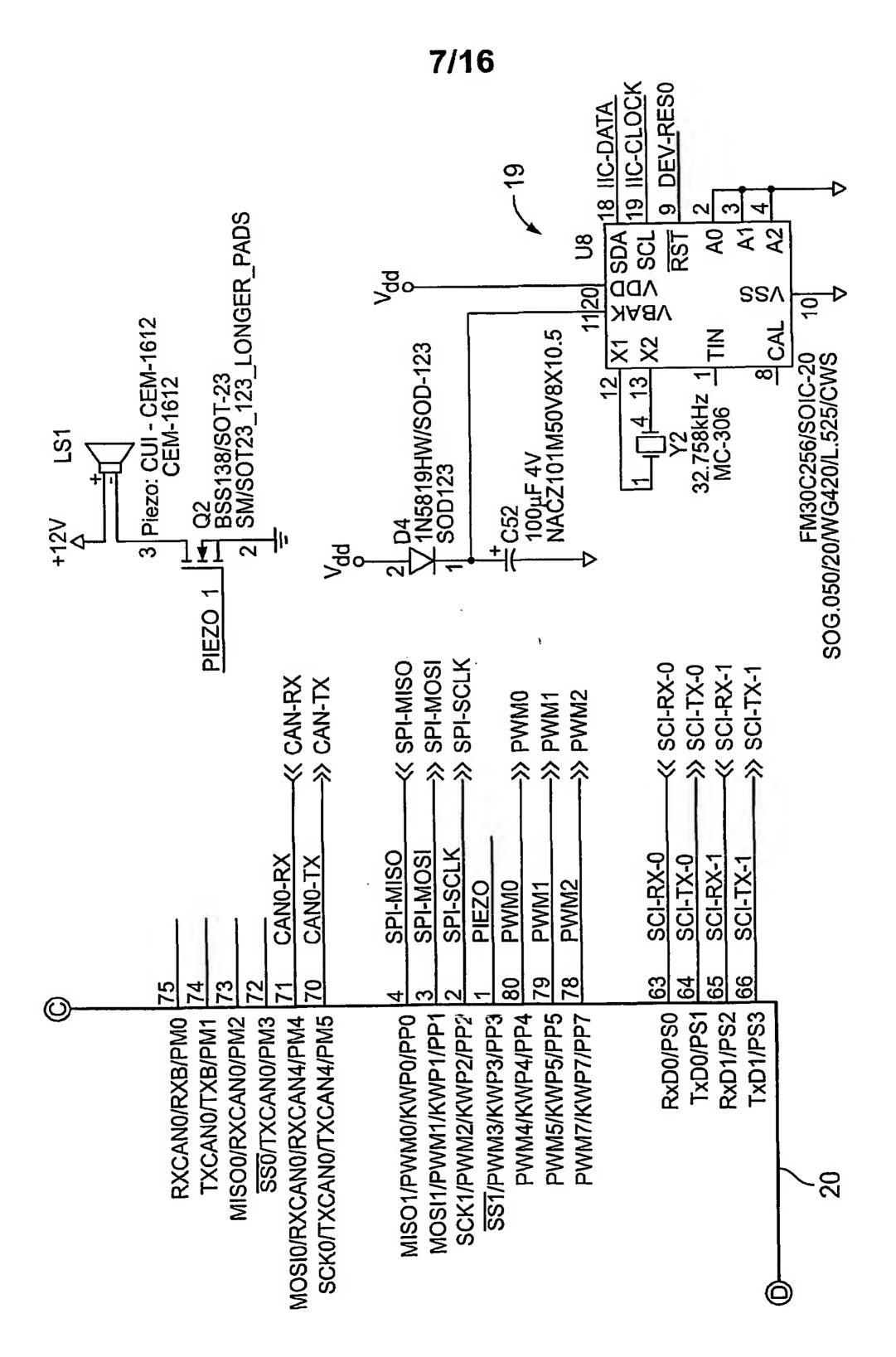
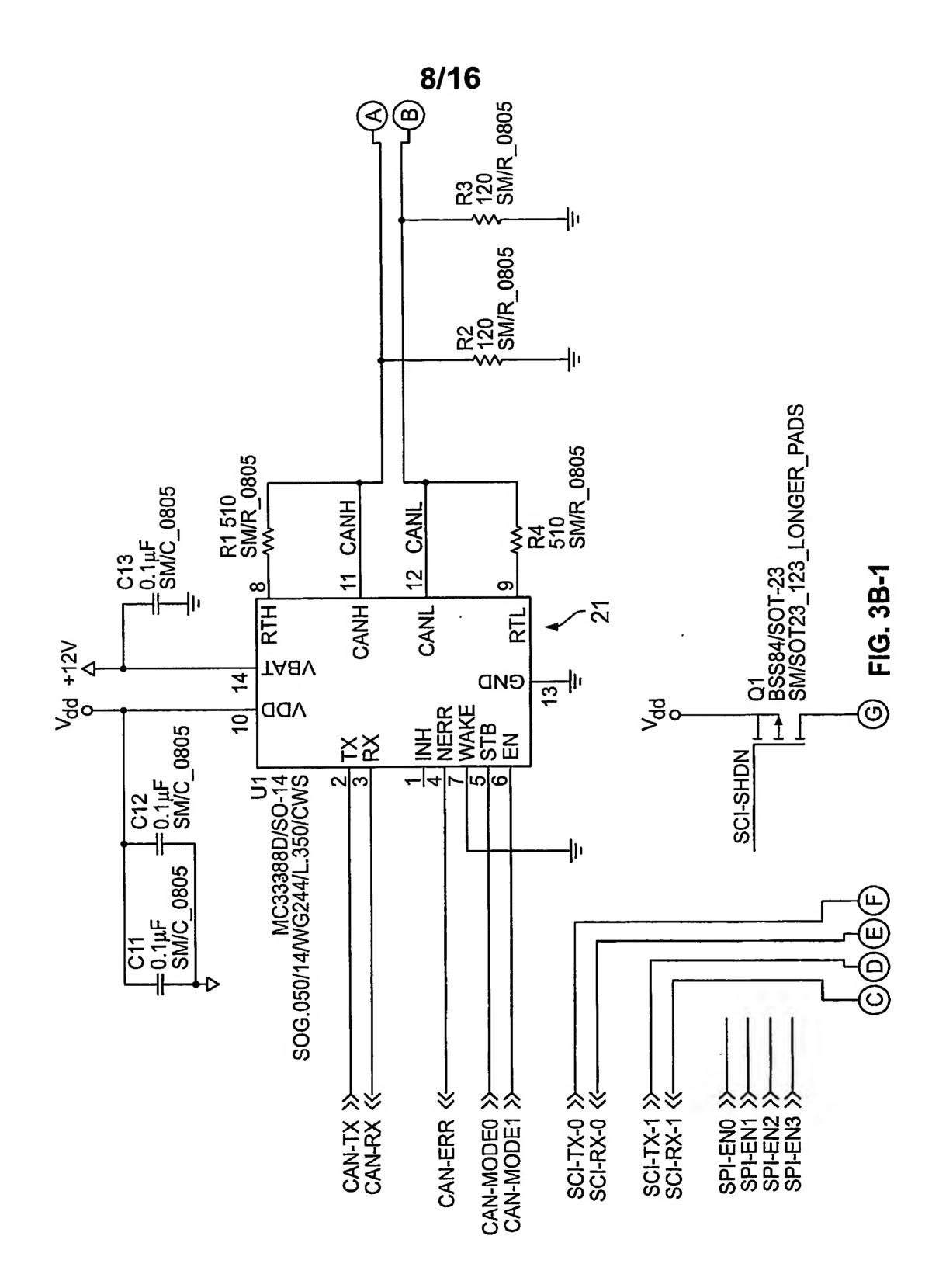
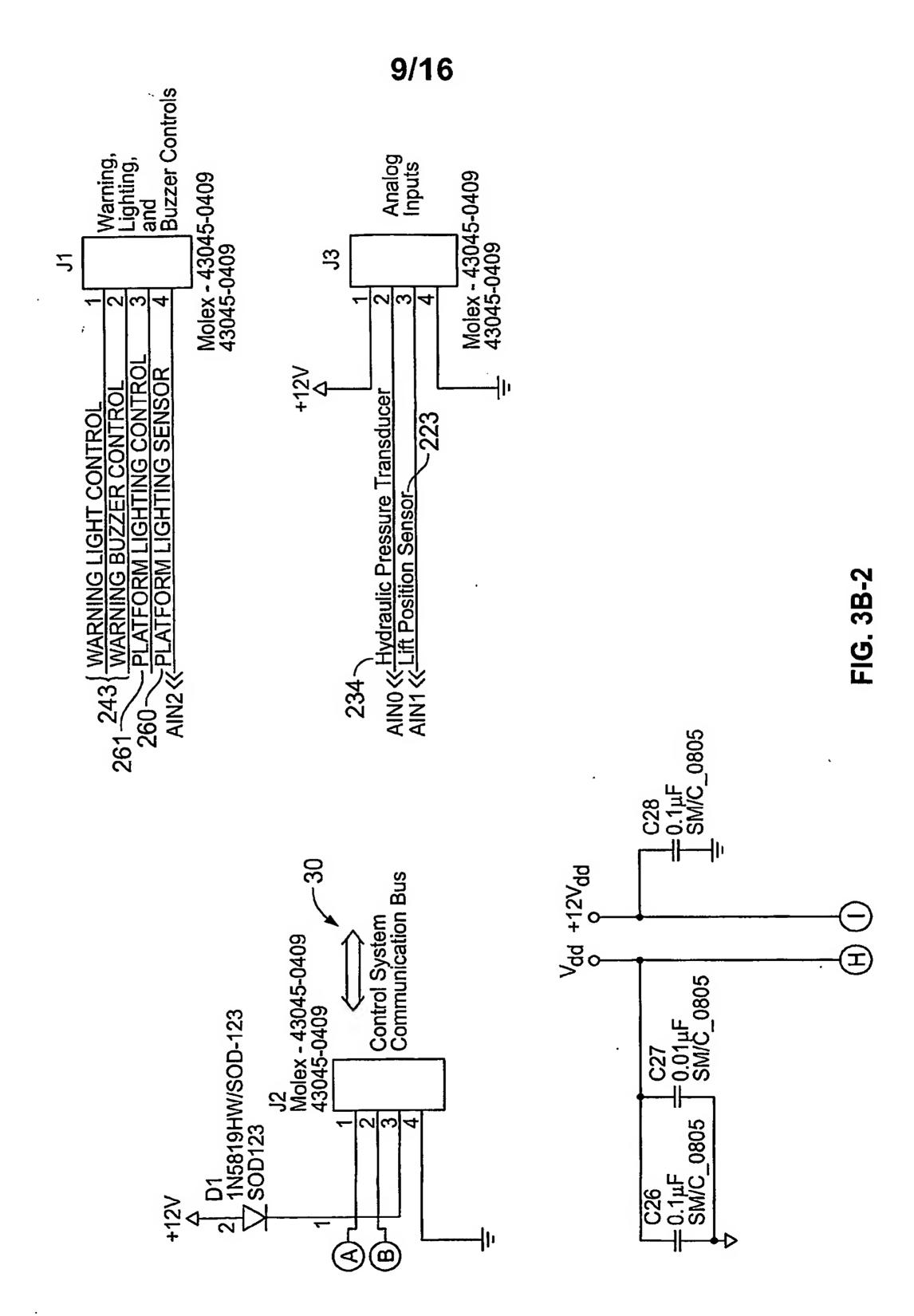
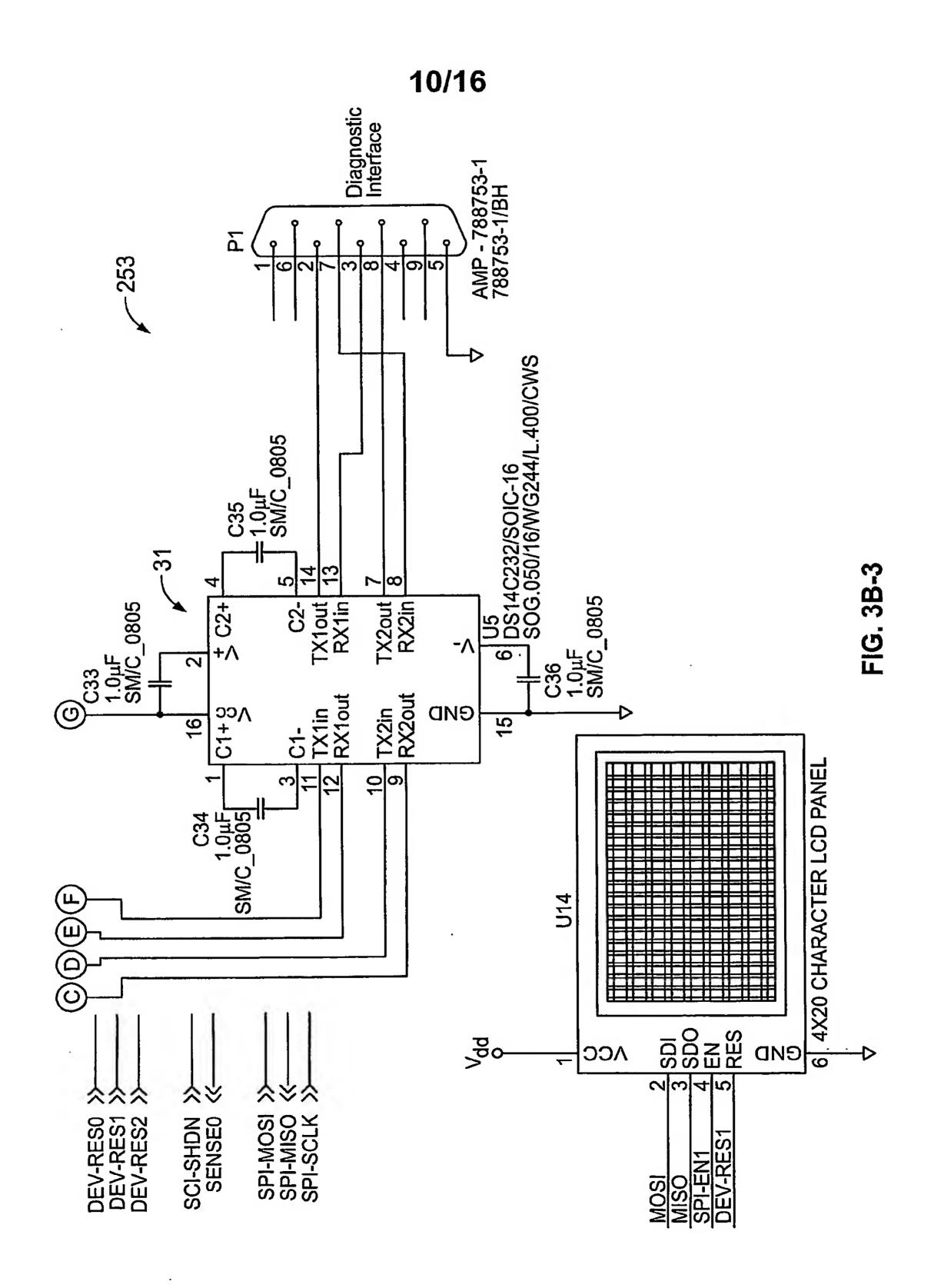
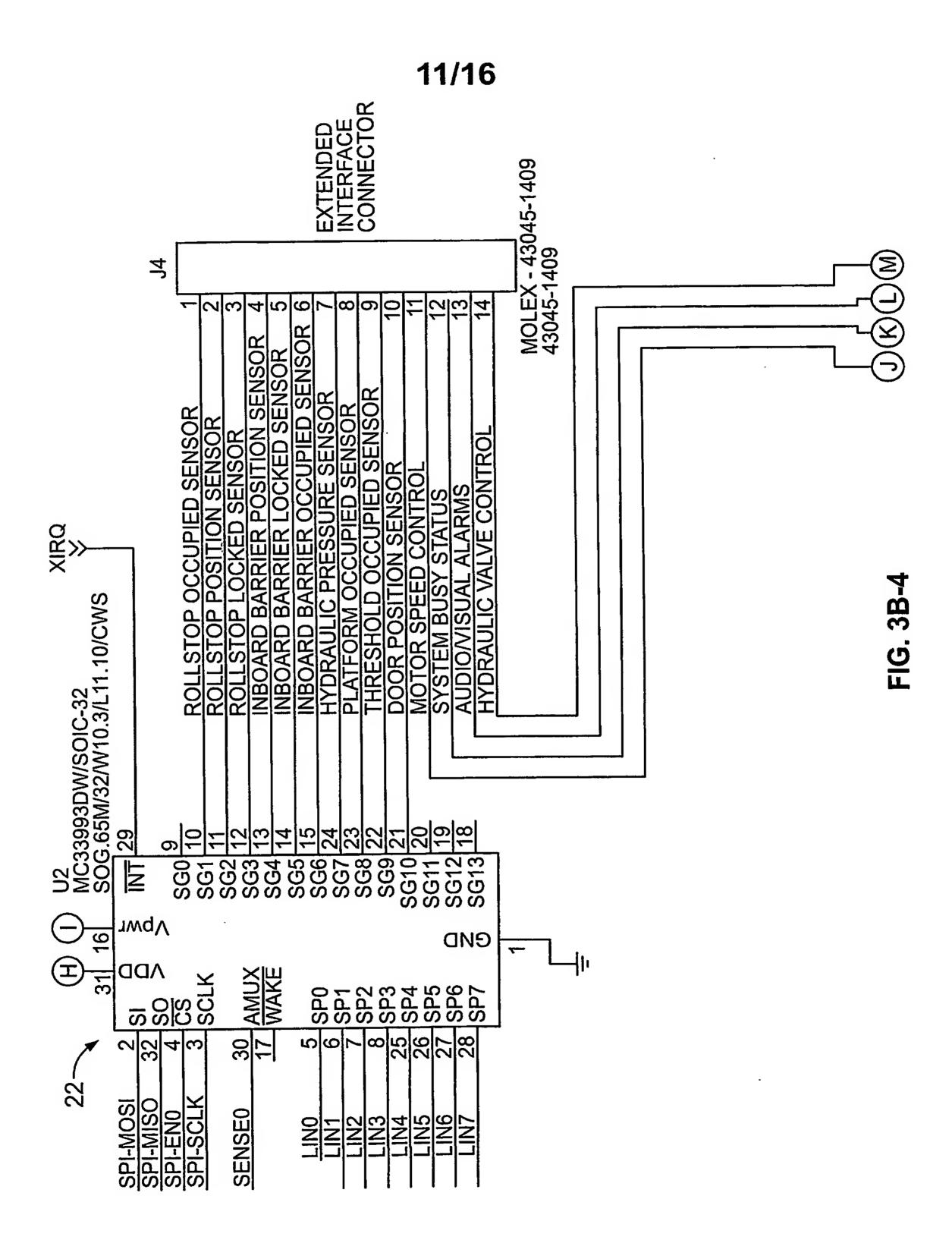


FIG. 3A-4









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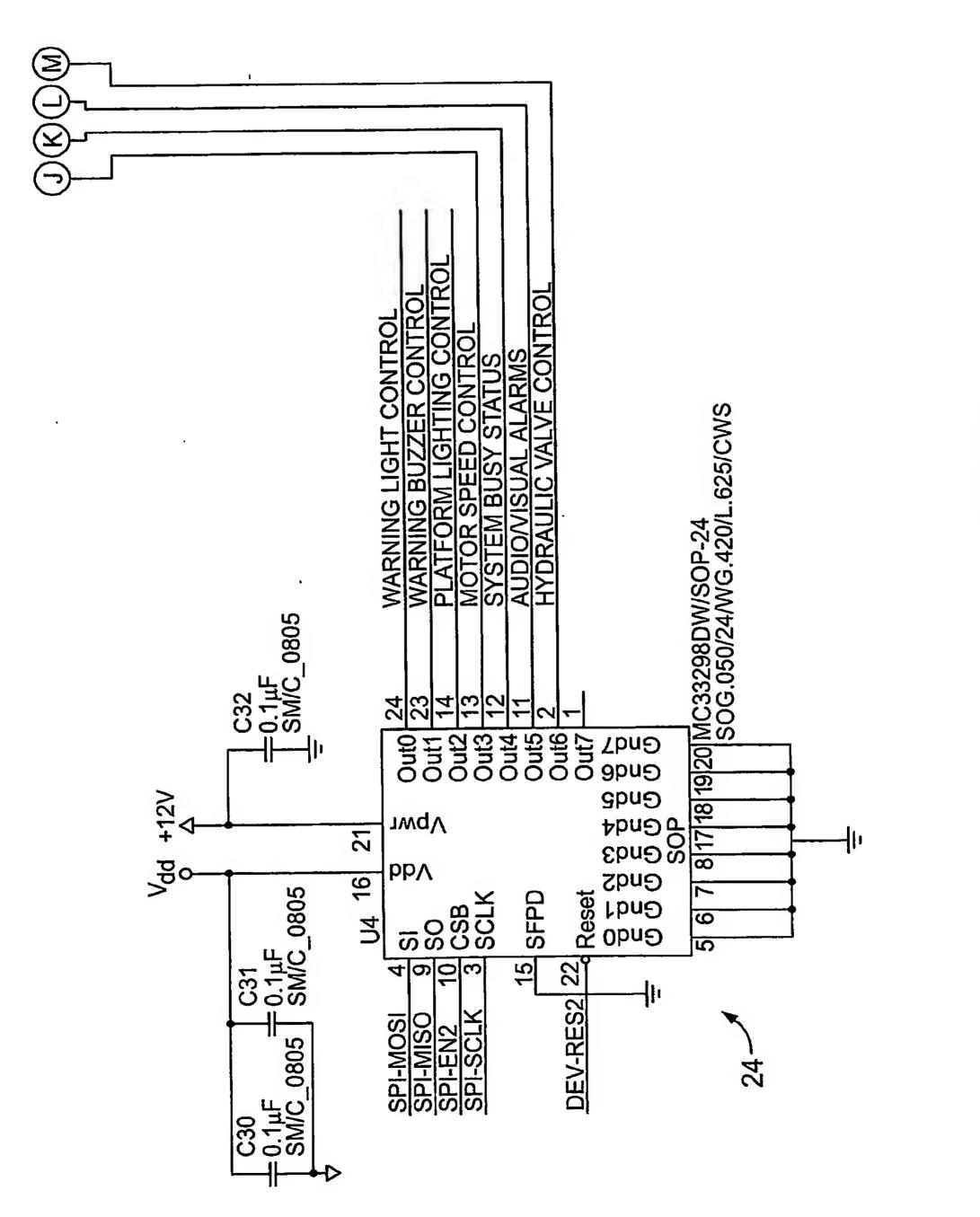
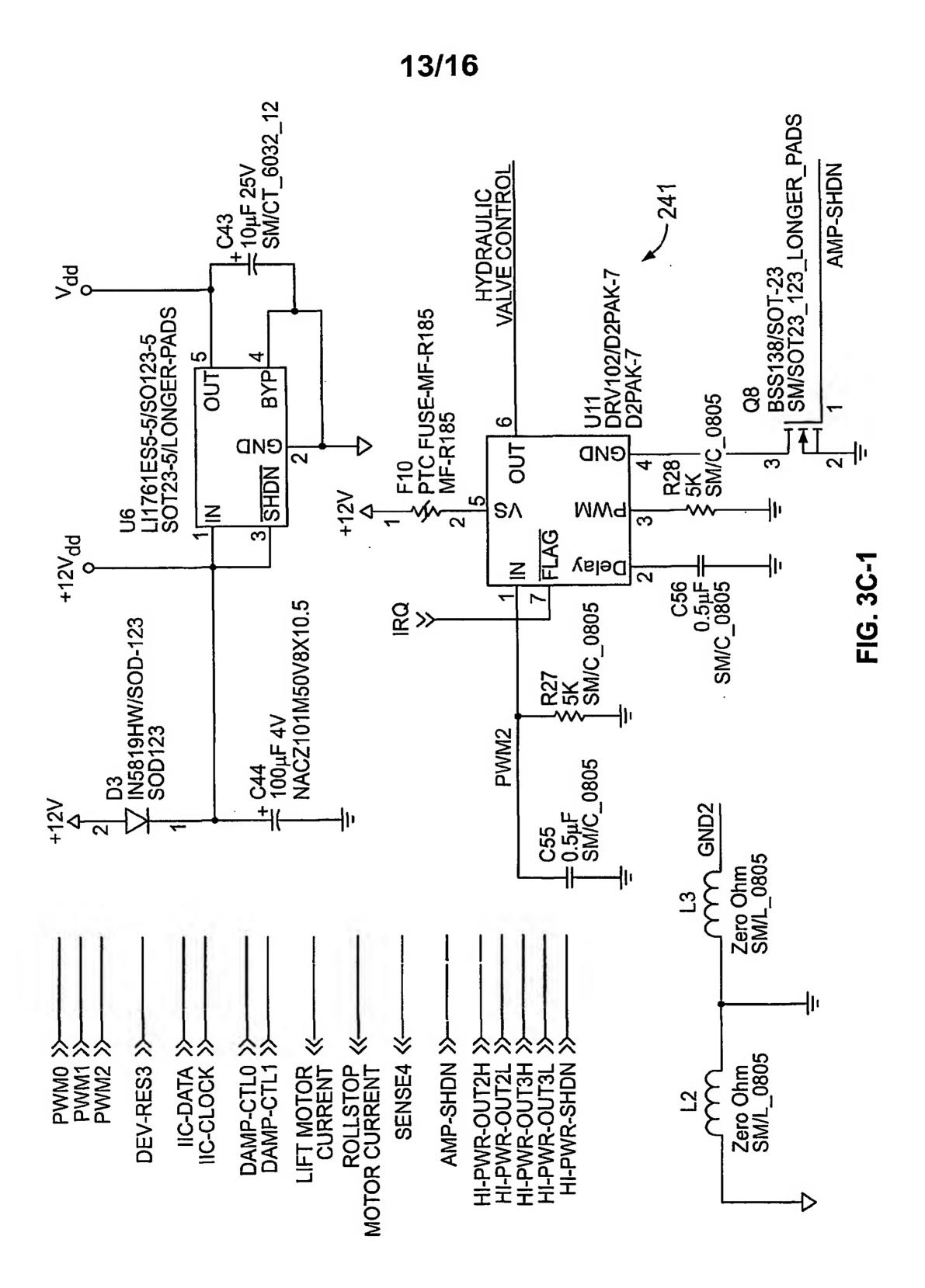
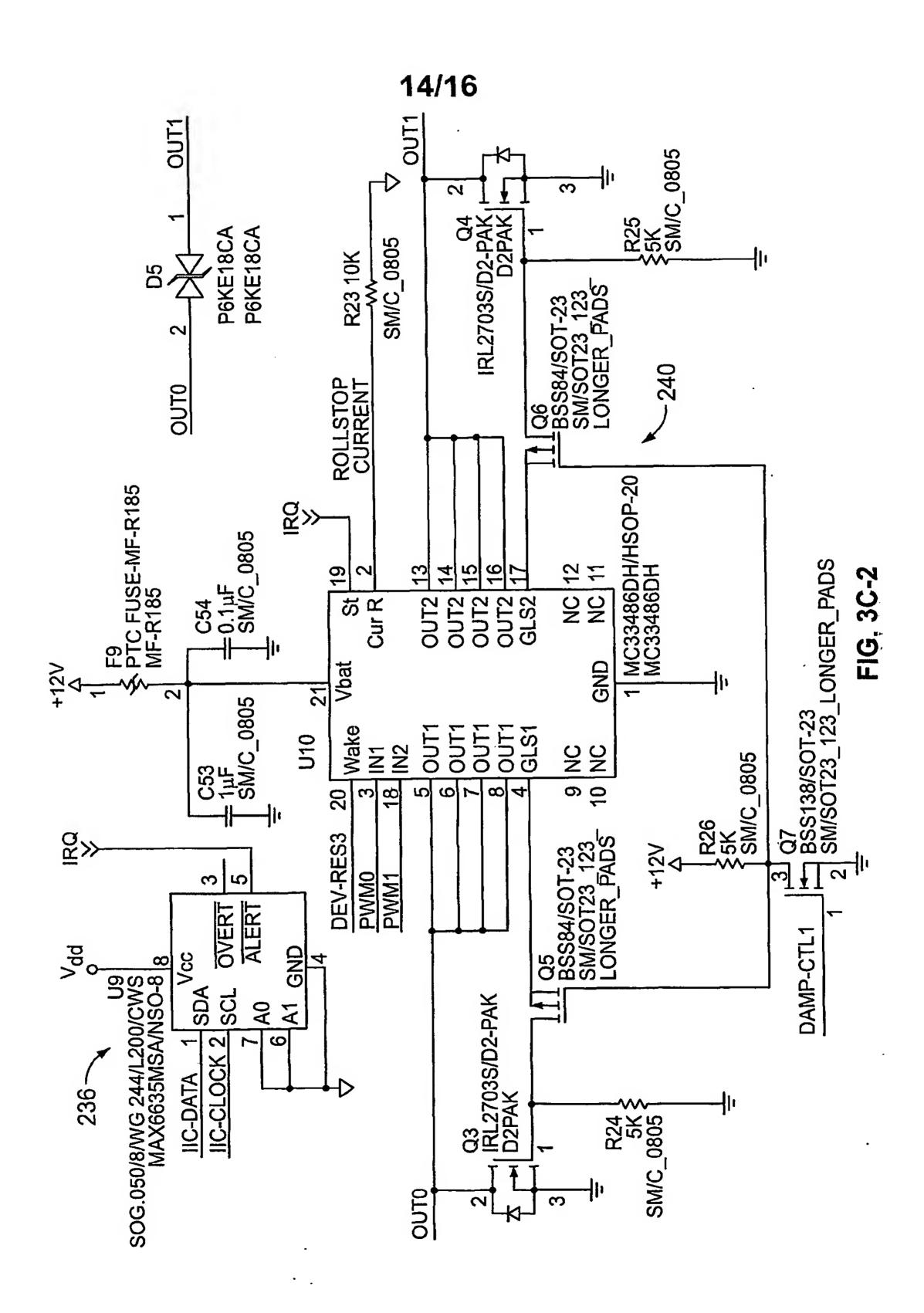


FIG. 3B-5

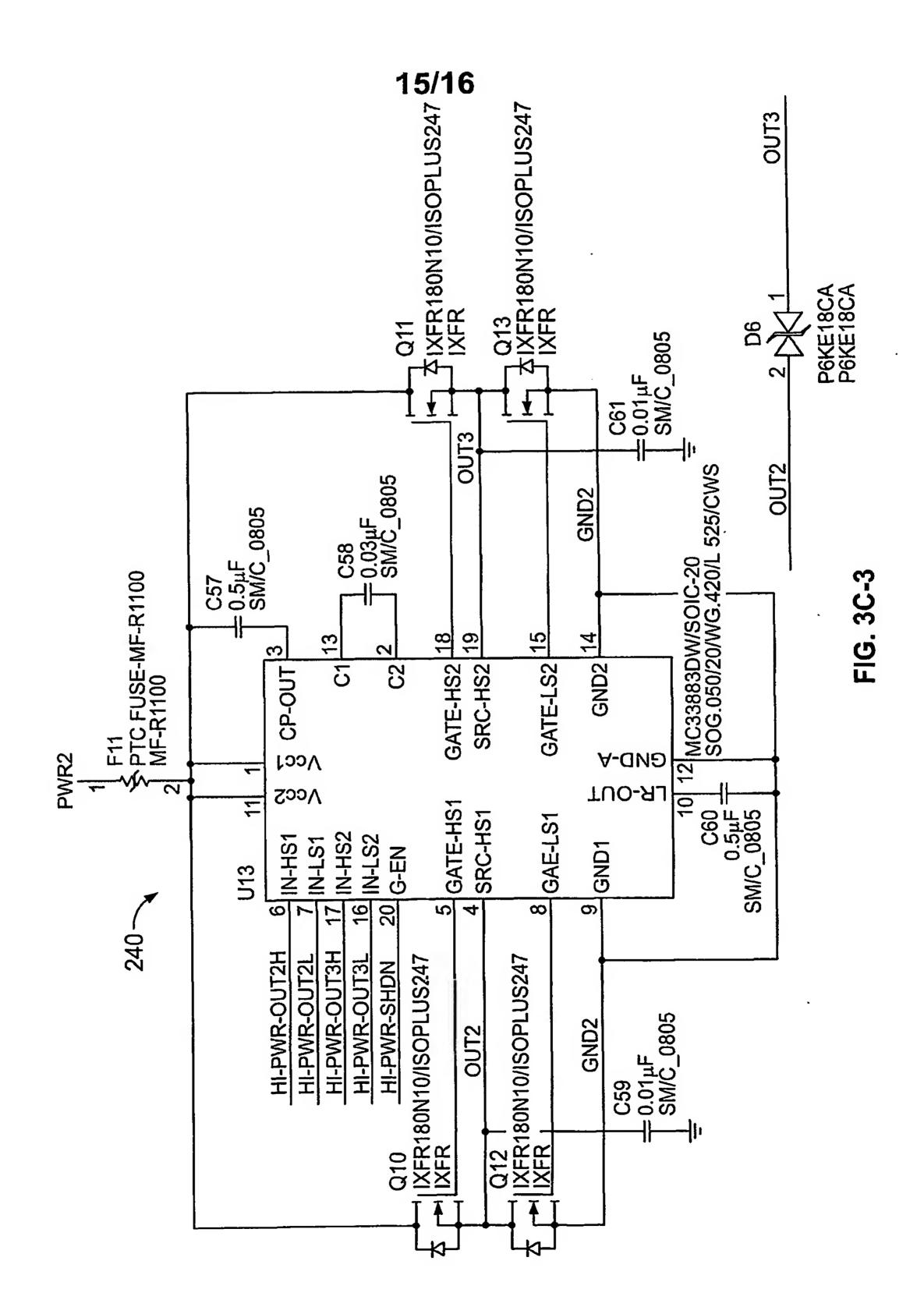


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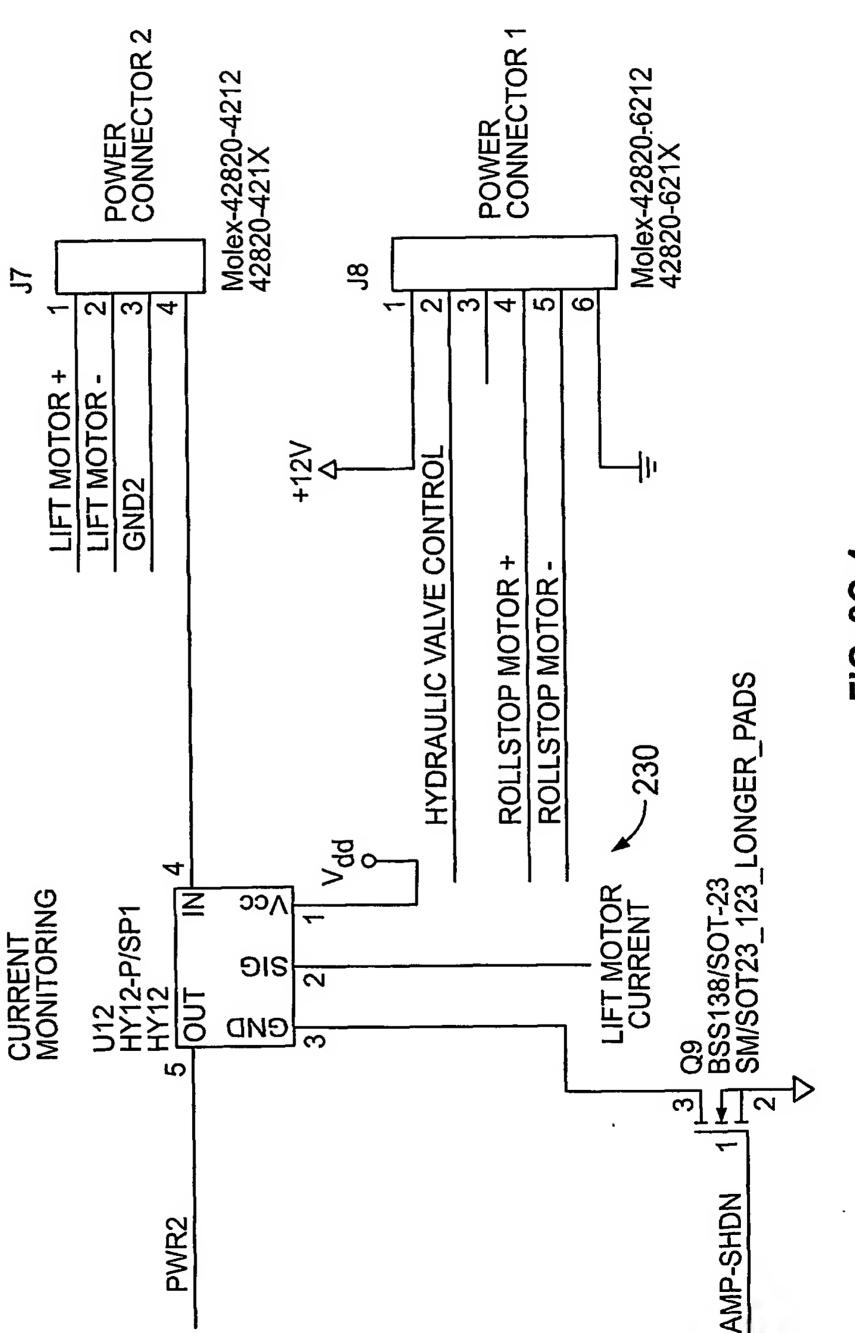


FIG. 3C-4